VE 427 VLSI Desgin

Summer 2021

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Canvas Pages:

1. https://umjicanvas.com/courses/2165

Office Hours: After class, or by email appointment, or post your questions in Feishu groups.

Main References: This is a restricted list of various interesting and useful books that will be touched during the course. You need to consult them occasionally.

- Jan Rabaey, *Digital Integrated Circuits: A Design Perspective*.
- John P. Uyemura, *Introduction to VLSI Circuits and Systems*.
- More to be updated throughout the semester.

Objectives: This course is primarily designed for senior undergraduate students interested in integrated circuit design. We will cover the fundamentals and the tools for designing a real-life system.

Prerequisites: An undergraduate-level understanding of digital integrated circuits, such as VE 312, is expected. Understanding of devices is appreciated, such as VE 320. We will also review essential concept of semiconductors in the class.

Tentative Course Outline:

- A review of MOSFET, CMOS logic, basic memory blocks.
- A review of combinational logic, finite state machine, Verilog
- Architecture of FPGA
- Timing constraints
- Low-power designs
- RISC-V and stream processing
- Memory/ Cache
- Digital signal processing circuits
- I/O network
- Parallelism
- List processor optimization, VLIW compiler
- Techniques in adder/multiplier/shifters
- Clock and power distribution
- Research topics: DNN, highspeed wireline, etc.

Grading Policy: Assignments (40%), Midterm (15%), Final (15%), Final project (30%).

Important Dates:

Downloadable ebook versions are available on https://booksonweb.files.wordpress.com/2011/11/digital-integrated-circuits-a-design-perspective-by-jan-m-rabaey.pdf.

Midterm 6/23
Final 8/4
Final project report ..... due by 8/5

Assignments: Assignments include written Homework and Labs.

Homework1 ..... due by 5/24
Homework2 ..... due by 6/12
Homework3 ..... due by 7/19
Lab1 ..... due by 5/24
Lab2 ..... due by 6/21
Lab3 ..... due by 7/10

Class Policy: Regular attendance is encouraged.

Home Late Policy: 20% points deducted per day.

Academic Honesty: Lack of knowledge of the academic honesty policy is not a reasonable explanation for a violation.